



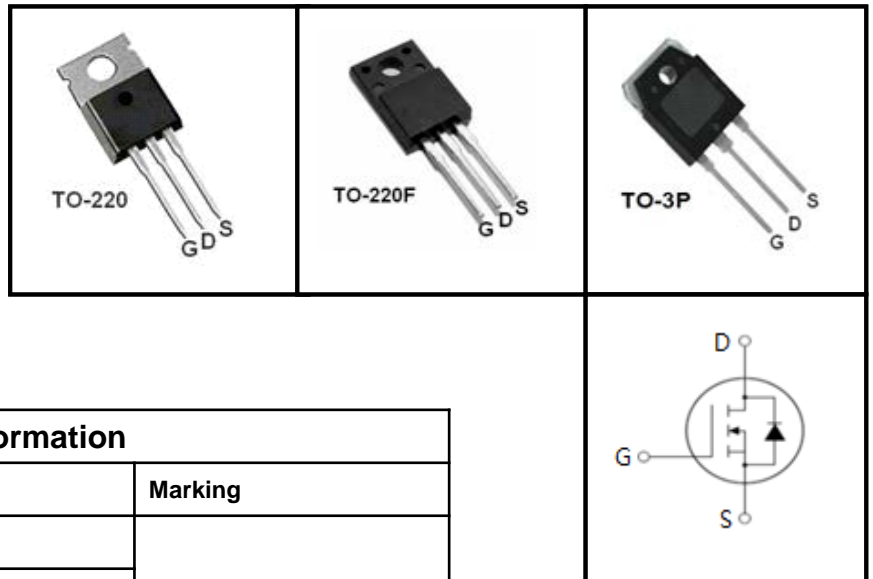
# 650V Super-Junction Power MOSFET

## FEATURES

- Very low FOM  $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



Device Marking and Package Information		
Device	Package	Marking
TPP65R210A	TO-220	65R210A
TPA65R210A	TO-220F	
TPV65R210A	TO-3P	

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , unless otherwise noted					
Parameter	Symbol	Value			Unit
		TO-220	TO-3P	TO-220F	
Drain-Source Voltage ( $V_{GS} = 0\text{V}$ )	$V_{DSS}$	650			V
Continuous Drain Current	$I_D$	20			A
Pulsed Drain Current (note1)	$I_{DM}$	60			A
Gate-Source Voltage	$V_{GSS}$	$\pm 30$			V
Single Pulse Avalanche Energy (note2)	$E_{AS}$	500			mJ
Avalanche Current (note1)	$I_{AR}$	10			A
Repetitive Avalanche Energy (note1)	$E_{AR}$	1			mJ
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	208		34.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150			$^\circ\text{C}$

Thermal Resistance					
Parameter	Symbol	Value			Unit
		TO-220	TO-3P	TO-220F	
Thermal Resistance, Junction-to-Case	$R_{thJC}$	0.6		3.6	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	62		80	



Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	$\mu A$
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	--	--	100	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10A$	--	0.19	0.21	$\Omega$
Forward Transconductance (Note3)	$g_{fs}$	$V_{DS} = 10V, I_D = 10A$	--	18.8	--	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	2140	--	$\mu F$
Output Capacitance	$C_{oss}$		--	300	--	
Reverse Transfer Capacitance	$C_{rss}$		--	18	--	
Total Gate Charge	$Q_g$	$V_{DD} = 480V, I_D = 20A,$ $V_{GS} = 10V$	--	54	--	nC
Gate-Source Charge	$Q_{gs}$		--	10	--	
Gate-Drain Charge	$Q_{gd}$		--	20	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 20A,$ $R_G = 25\Omega$	--	48	104	ns
Turn-on Rise Time	$t_r$		--	108	220	
Turn-off Delay Time	$t_{d(off)}$		--	176	360	
Turn-off Fall Time	$t_f$		--	50	108	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	20	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	60	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 20A, V_{GS} = 0V$	--	0.95	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R = 480V, I_F = I_S,$ $di_F/dt = 100A/\mu s$	--	440	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	5	--	$\mu C$
Peak Reverse Recovery Current	$I_{rrm}$		--	24	--	A

**Notes**

1. Repetitive Rating: Pulse Width limited by maximum junction temperature
2.  $I_{AS} = 10A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse Width  $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics

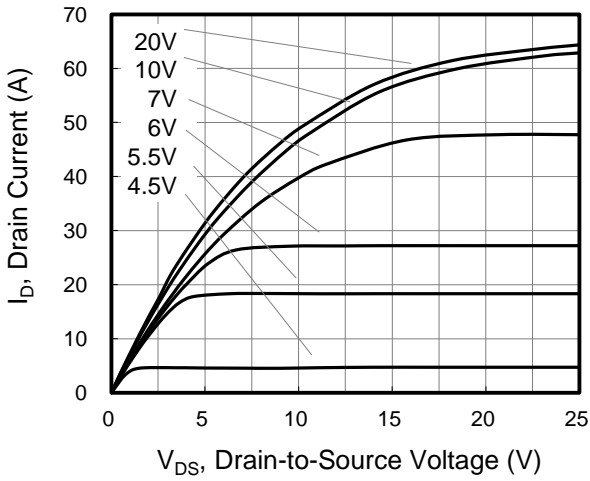


Figure 2. Transfer Characteristics

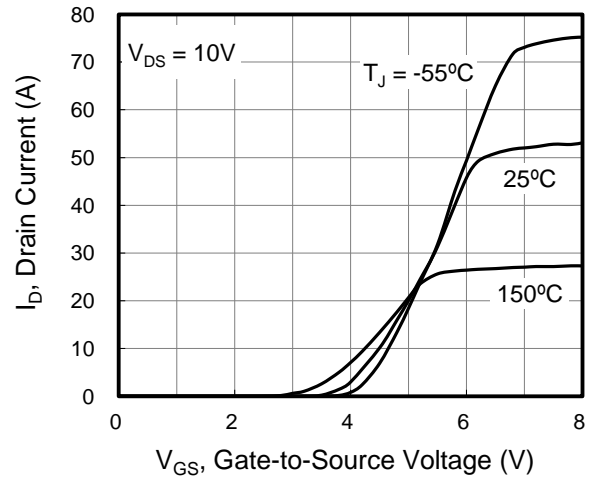


Figure 3. On-Resistance vs. Drain Current

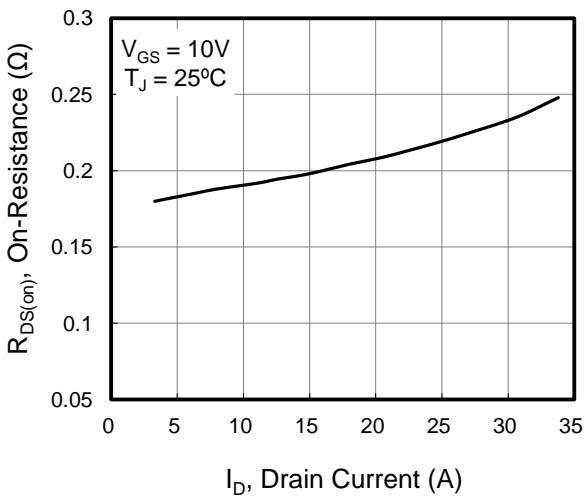


Figure 4. Capacitance

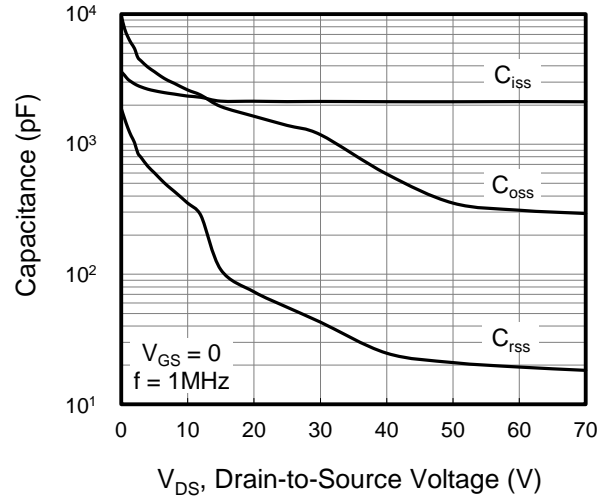


Figure 5. Gate Charge

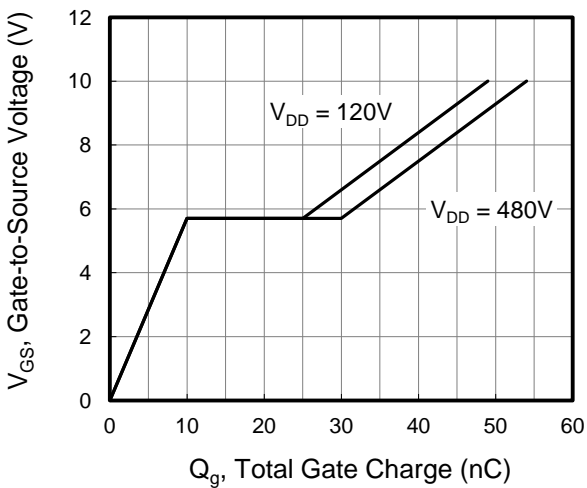
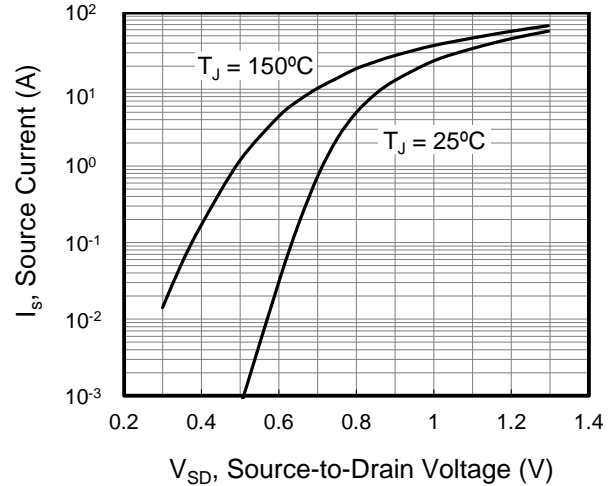


Figure 6. Body Diode Forward Voltage





Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. On-Resistance vs. Junction Temperature

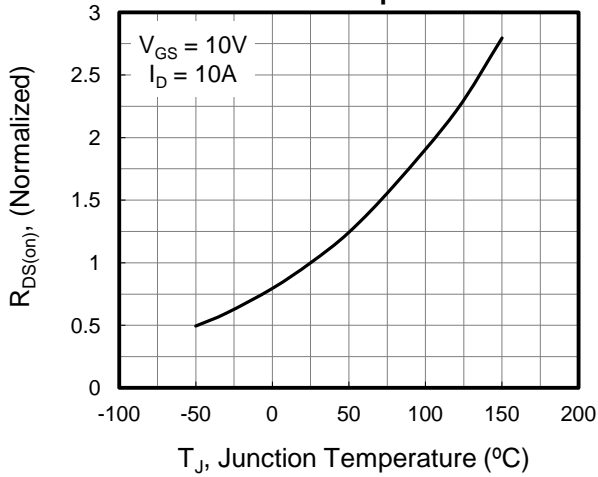


Figure 8. Threshold Voltage vs. Junction Temperature

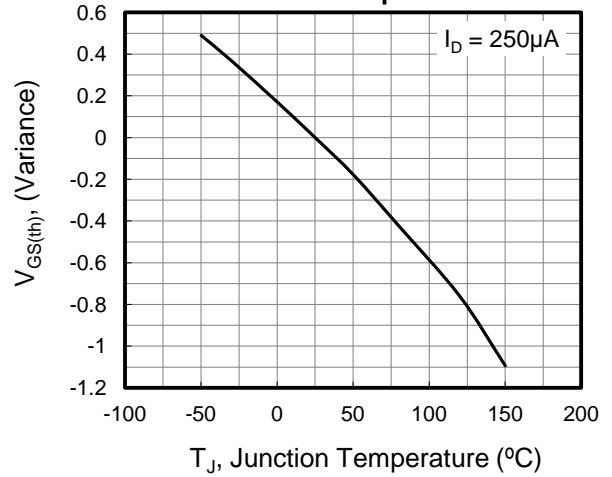


Figure 9. Transient Thermal Impedance TO-220/TO-3P

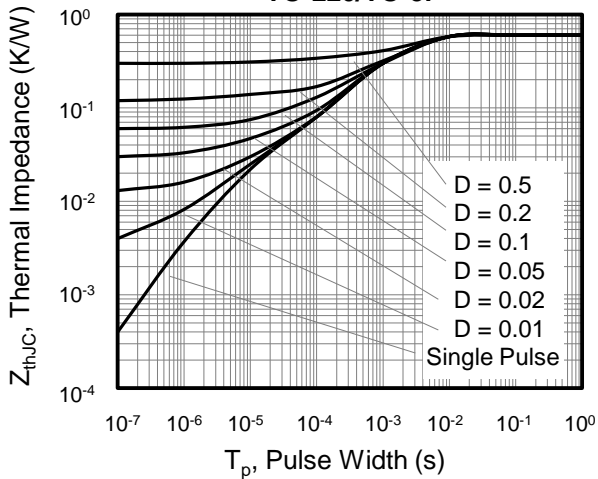


Figure 10. Transient Thermal Impedance TO-220F

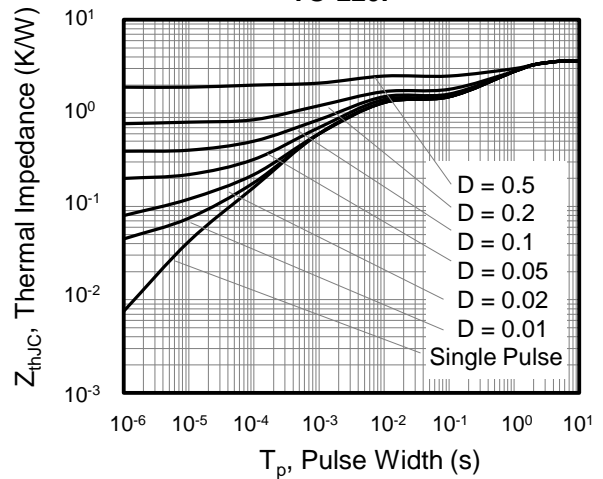


Figure 11. Safe Operating Area TO-220/TO-3P

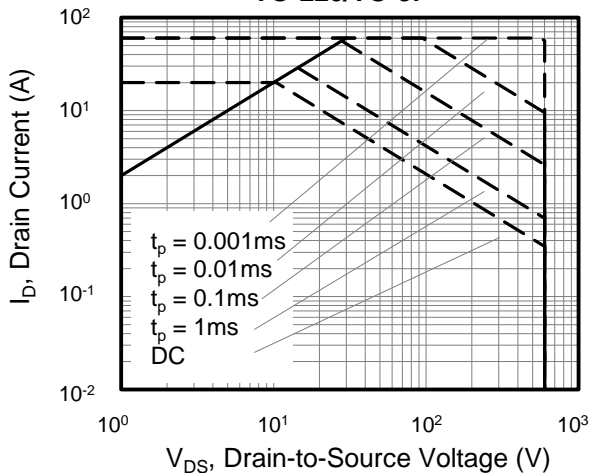


Figure 12. Safe Operating Area TO-220F

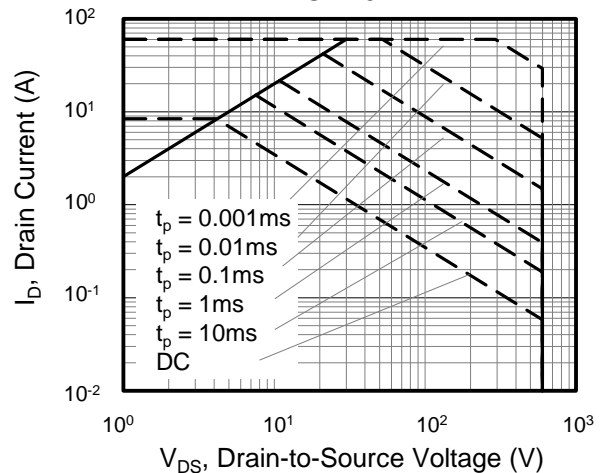




Figure A: Gate Charge Test Circuit and Waveform



Figure B: Resistive Switching Test Circuit and Waveform

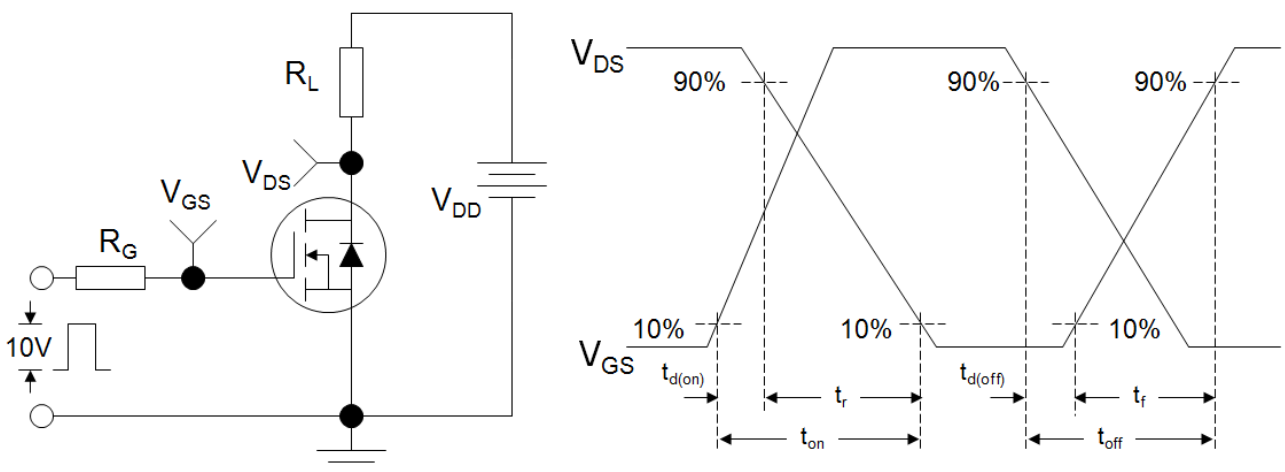
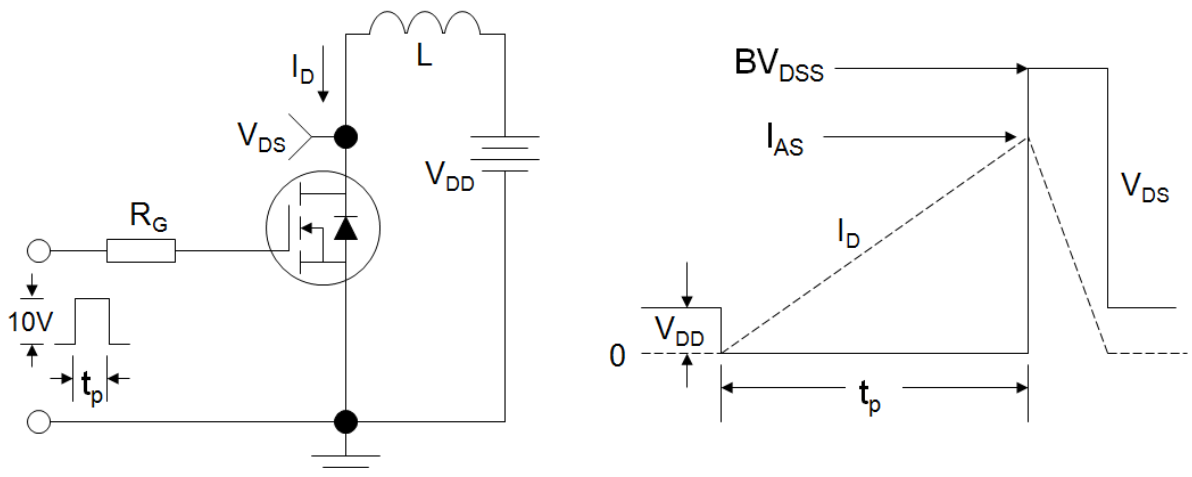


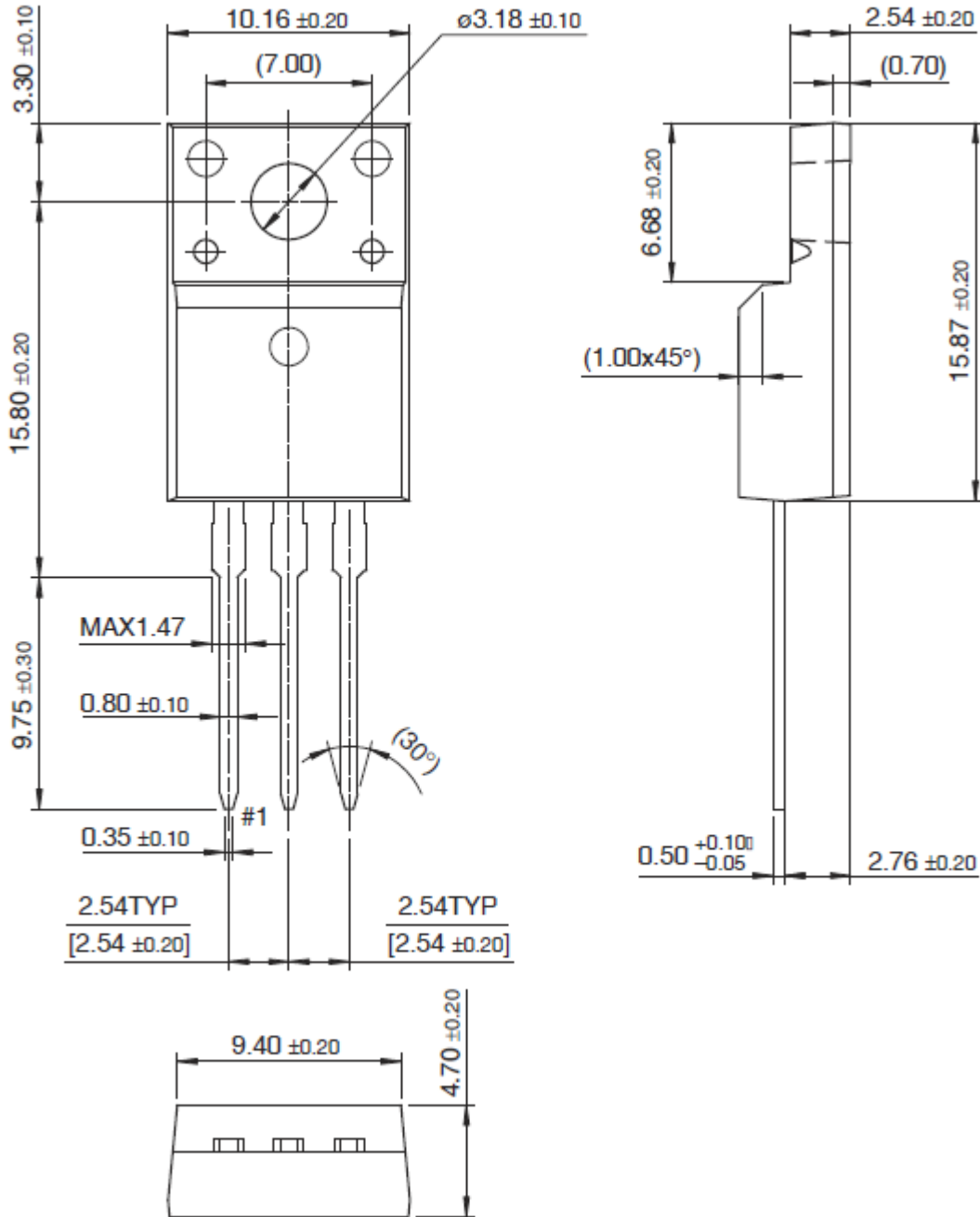
Figure C: Unclamped Inductive Switching Test Circuit and Waveform





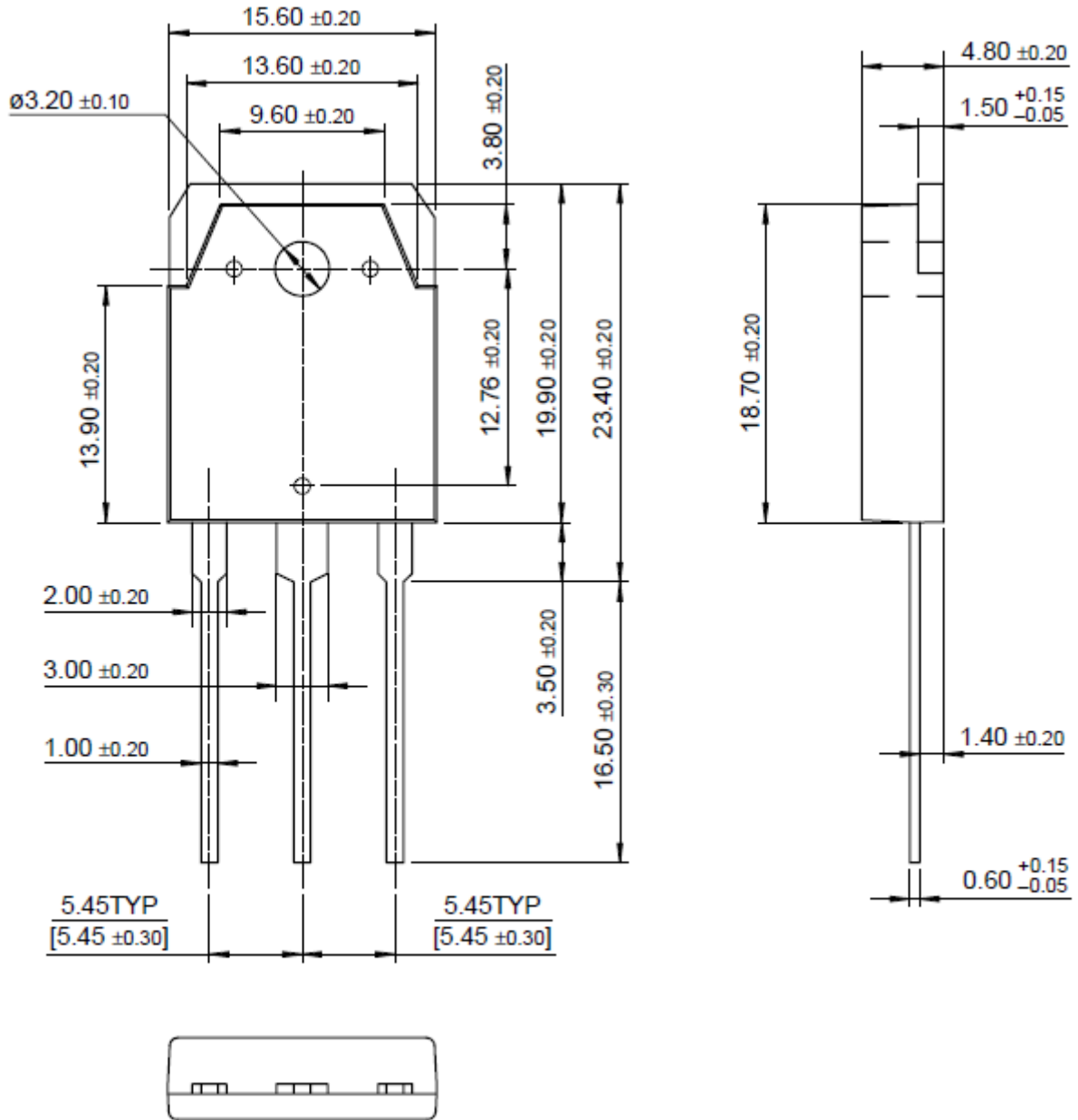


### TO-220F





### TO-3P







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